PATENT ABSTRACTS OF JAPAN

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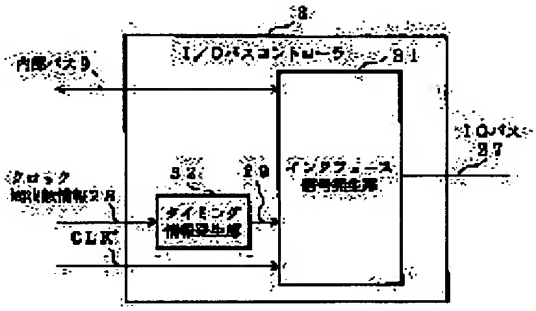
(54) COMPUTER SYSTEM

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce power consumption without reducing the processing speed of an extended device by controlling the change timing of an interface signal.
SOLUTION: A clock supply part sets up reference clock frequency lower than normal frequency and transmits the set clock frequency information 28 to an I/O bus controller 8. A timing information generation part 32 in the controller 8 recognizes current clock frequency from the inputted information 28, calculates timing information 29 for changing an interface signal by converting the information into clock frequency and transmits the information 29 to an interface signal generation part 31. The generation part 31 prepares an interface signal on the basis of the information 29 and accesses an extended device, e.g. KBCont.



LEGAL STATUS

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